DESCRIPTIONS OF IC'S USED IN DIGITAL LABS (ic_specs.doc jgl 11/25/12)

(These do not include gate chips: 7400, 02, 04, 08, 10, 32, and 86. Notational note: on the Standard IC Symbol sheet, a "bubbled" pin indicates an active-low input or output. Here, a "/" preceding the pin name means the same thing. Thus, /CLR = $\overline{\text{CLR}}$. This specifically refers to the voltage *at the pin*. Inside the symbol--on the other side of the bubble from the pin--it would be shown as CLR.)

7470: AND-GATED J-K FLIPFLOP. This flipflop is positive-edge triggered (rising edge of clock CLK). It has active-low asynchronous preset and clear inputs, /PRE and /CLR:

/PRE = 0 (low voltage at pin 13) forces Q $\rightarrow$ 1 asynchronously.

/CLR = 0 (low voltage at pin 2) forces Q $\rightarrow$ 0 asynchronously.

(Note: make sure CLK is low before activating either /PRE or /CLR. If the latter are not used, they should be "tied high"--connected to 5V--preferably through a pull-up resistor.)

This flipflop has two sets of J-K inputs: J1, J2, /J and K1, K2, /K. Inputs /J and /K are active-low and must be grounded if not used. The flipflop's internal J is the AND of the 3 external J's; i.e. J(int) = (J1 • J2 • /J). Thus J(int) $\rightarrow$ 1 when J1 = 1, J2 = 1, and /J = 0. The flipflop's internal K works the same way.

7474: DUAL D-TYPE FLIPFLOPS. This chip contains two positive-edge triggered D-flipflops with separate active-low preset and clear inputs (see notes on PRE and CLR under "7470".) The clock inputs are also separate. Clocking is done on the rising edge of the clock voltage: or

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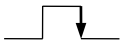
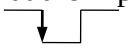
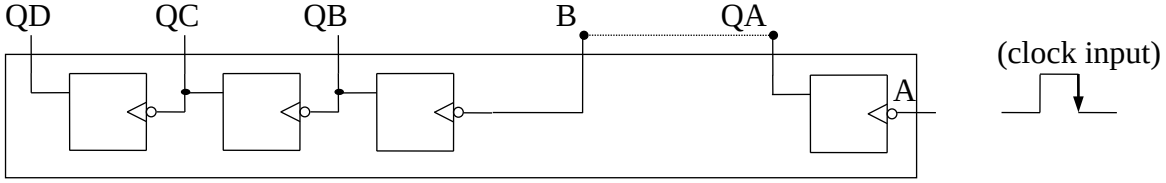
7476: DUAL JK-FLIPFLOPS. This chip is similar to the 7474 except that the flipflops are J-K. Another difference is that the clocks trigger on the negative edge:  or 

7483: 4-BIT BINARY ADDER WITH FAST CARRY. This chip contains a fast "look-ahead" carry circuit which eliminates ripple delay associated with a chain of identical full adders. It adds two 4-bit inputs, A = A4,A3,A2,A1 and B = B4,B3,B2,B1 plus an input carry, C0. It outputs 4 sum bits S = S4,S3,S2,S1 and an output carry, C4, such that S = A + B + C0, and C4 = 1 if sum overflows.

7493: 4-BIT BINARY ASYNCHRONOUS (RIPPLE) COUNTER. This chip contains four J-K flipflops. Each one has J=K=1 and toggles (changes state) whenever it is clocked. Flipflops D, C, and B are chained together internally as a 3-bit ripple counter (D is msb--see figure). Each flipflop is clocked when the output of the previous flipflop falls (negative-edge triggering). In response to a series of clock pulses at input-B, DCB cycles through the binary count: 000 $\rightarrow$ 001 $\rightarrow$ 010 $\rightarrow$ 011 $\rightarrow$ ... 111 $\rightarrow$ 000 ...

Flipflop A is independent of the others. It is clocked on the falling edge of the voltage at input-A, and toggles each time it is clocked. To create a 4-bit counter, flipflop A must be added to the chain so that flipflop B toggles on the falling edge of QA. This connection must be made externally (dotted line).



In additon, the 7493 has two asynchronous active-high reset inputs, R0(1) and R0(2), pins 2 and 3. These

7493 (continued):

inputs are ANDed internally and brought to the clear inputs (not shown) of the 4 flipflops. In order to reset the count and make DCBA → 0000, *both* of these reset inputs must go high at the same time. When one or both go low, the chip will resume counting. (Note: use the standard IC symbol for the 7493 in circuit diagrams, not the internal view of the 7493 shown above.)

74151: 8-TO-1 MULTIPLEXER (i.e. 1-OF-8 DATA SELECTOR). This MUX has eight data inputs, D7...D0, three select inputs C,B,A (C is msb), a normal output Y, and an inverted output W. There is also an active-low enable, or Gate, input /G.

When /G is high, output Y stays low (0), and W stays high (1), regardless of which input is being selected. When /G is low, Y equals the selected input (and W its complement). Thus, for CBA = 100, Y = D4 and W = /D4, etc..

74155: 3X8 OR DUAL 2X4 DECODER. This IC can be used in two ways. As a dual 2x4 decoder, it can be thought of as separate decoders with common select inputs B,A. Since the select inputs are common, the decoders are not really independent, and as such, they are of limited usefulness. The really utility of this chip for decoding (rather than demultiplexing) purposes is as a 3x8 decoder.
The enable inputs for the 3x8 configuration are /1G (pin 2) and /2G (pin14). These active-***low*** inputs must *both* be low for the decoder to operate. If either or both are high, then all 8 outputs go inactive. To operate the decoder continuously, just ground both /1G and /2G.

The decoder needs a third select input, in addition to B and A. This is formed by connecting the inputs 1C and 2C together and calling the result "C". The select inputs are now CBA (with C the msb).

The 8 outputs will be designated Y7...Y0. These are related to pin numbers as follows:

Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	(3x8 outputs)
4	5	6	7	12	11	10	9	(pin numbers)

Standard pin labels (1Y3...1Y0, 2Y3...2Y0) shown on the 74155 diagram are confusing when the 74155 is used as a 3x8 decoder. To avoid confusion, just ignore them and rely only on pin numbers to identify decoder outputs (as shown above). These decoder outputs are active LOW. Thus, if the decoder is enabled and select inputs are CBA = 011, then Y3 → 0, while the 7 outputs that are not selected remain high; i.e.

Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
H	H	H	H	**L**	H	H	H

If the decoder is not enabled (either /G1 or /G2 or both are high), then all Y's stay high.

74157: QUAD 2-TO-1 MULTIPLEXER. The 74157 consists of four 2-to-1 MUX's, each with an A and B data input, and an output Y (e.g. inputs = 2A,2B; output = 2Y). The standard IC symbol reflects this internal MUX structure. However, in digital labs, the 74157 is used as a data selector; it chooses between two 4-bit numbers, (4A...1A) and (4B...1B). Therefore, circuit diagrams would probably be clearer if the IC symbol had grouped the A's and B's as separate input sets. (It would also have been helpful if subscripts were consistent with textbook notation; e.g. A3...A0 instead of 4A...1A.) In addition, this chip has a control input which selects between the 2 input sets; its symbol is A/B.

74157 (continued):

When low, it selects the A's: (4A...1A) → (4Y...1Y).
When high, it selects the B's: (4B..1B) → (4Y...1Y).

Finally, there is an active-low enable (or Gate) input, /G. When this is high (inactive), then all outputs go low: (0...0) → (4Y...1Y), and the select input is ignored.

74161: SYNCHRONOUS 4-BIT BINARY COUNTER WITH PARALLEL LOAD. This is a register-counter with 4 flipflops. Outputs are QD...QA (where QD is msb). There is also a 5th output, RCO = Ripple Carry Output, described below. In addition, there are 4 data inputs, D...A (msb is D), an asynchronous active-low clear input /CLR, an active-low load input /LOAD, a positive-edge triggered clock, plus 2 count-enable inputs ENT and ENP which are internally ANDed. The effects of these inputs are shown in the
following function table. (Note: EN = ENT•ENP.)

	/CLR	/LOAD	EN	CLK	FUNCTION
1	L	X	X	X	CLEAR: (0000) → (QD...QA).
2	H	H	L	X	HOLD (no change).
3	H	L	X	↑	LOAD: (D...A) → (QD...QA).
4	H	H	H	↑	COUNT UP.

Line 1 shows that /CLR has highest priority. When it is active, all other inputs are ignored. Line 3 shows that /LOAD is second in priority; when it is active, EN (count enable) is ignored. Line 4 shows that counting takes place only when /LOAD is inactive and EN is high. Since EN represents an internal ANDing of inputs
ENT and ENP, *both* inputs must be high for counting to be enabled.

With counting enabled, the count QD...QA increases with each clock until it reaches 1111. The next clock rolls the count over to 0000. While the count is at 1111, the RCO output goes high. In a multi-stage counter, which consists of a chain of 74161's, the RCO of one chip would be connected to ENT and ENP of the next. When RCO = 1, it enables the next chip to increment when the clock comes. Since RCO goes low after the clock, the next chip won't increment again until the first chip goes through another cycle of 16 clocks and RCO goes high again.

It is important, when changing inputs /LOAD, ENT, and ENP, to make sure the clock is high when the changes take place--otherwise, problems might arise. If the clock comes from a pushbutton switch, keep the switch depressed while making changes in any of these inputs.

74179: 4-BIT SHIFT REGISTER WITH PARALLEL LOAD. This chip has 3 synchronous modes: shift right, parallel load, and hold (do nothing). The 74179 consists of 5 outputs: QA...QD, plus /QD. It has an active-low, asynchronous clear /CLR, 4 parallel data inputs A...D, a serial data input SER, a negative-edge clock CLK, and two active-high control inputs SHIFT and LOAD. The following function table shows the effects of these inputs:

	/CLR	LOAD	SHIFT	CLK	FUNCTION
1	L	X	X	X	CLEAR: (0000) → (QA...QD).
2	H	L	L	X	HOLD: (no change).
3	H	X	H	↓	SHIFT: (SER,QA,QB,QC) → (QA,QB,QC,QD).
4	H	H	L	↓	LOAD: (A...D) → (QA...QD).

74179 (continued)

Line 1 shows that /CLR has highest priority--when it is active, QA...QD all go low, and all other inputs are ignored. Line 3 shows that SHIFT has a higher priority than LOAD. (Note: this is a shift-right register if QA is considered the msb.)

74194: 4-BIT BIDIRECTIONAL SHIFT REGISTER WITH PARALLEL LOAD. The '194 has 4 synchronous modes: shift right, shift left, parallel load, and hold (do nothing). It consists of 4 outputs, QA...QD, plus 4 parallel data inputs A...D, and 2 serial inputs IR and IL. It also has an active-low asynchronous clear /CLR, a positive-edge triggered clock CLK, and 2 control inputs S1 and S0. Following is the function table for the 74194:

/CLR	S1	S0	CLK	FUNCTION
L	X	X	X	CLEAR: (QA...QD) <= (0000).
H	L	L	X	HOLD (no change).
H	L	H	↑	SHIFT RIGHT: (QA,QB,QC,QD) <= (IR,QA,QB,QC).
H	H	L	↑	SHIFT LEFT: (QA,QB,QC,QD) <= (QB,QC,QD,IL).
H	H	H	↑	LOAD: (QA...QD) <= (A...D).

/CLR has highest priority. When it is active, it clears the register immediately, without regard to the clock or any other inputs.

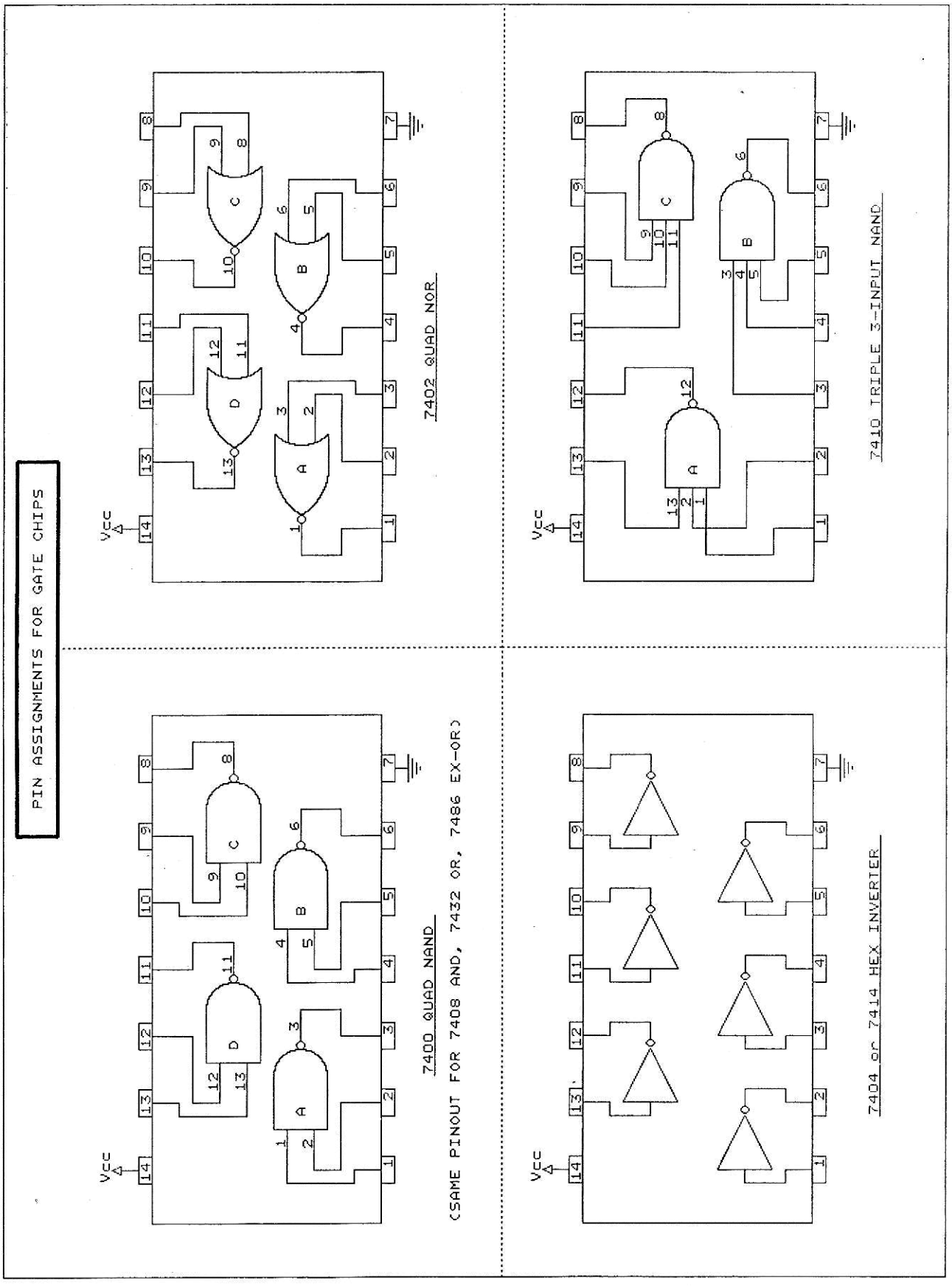
74195: 4-BIT SHIFT REGISTER WITH PARALLEL LOAD. This chip is similar in some ways to the 74179. It has the same 5 outputs, QA...QD, and /QD, shifts right only (QA → QD), and has an active-low clear /CLR. On the other hand, CLK is positive-edge triggered, and there is only 1 control input, $S/\overline{L}$ (Shift/Load), which causes shifting when high and loading when low. There is no HOLD state.

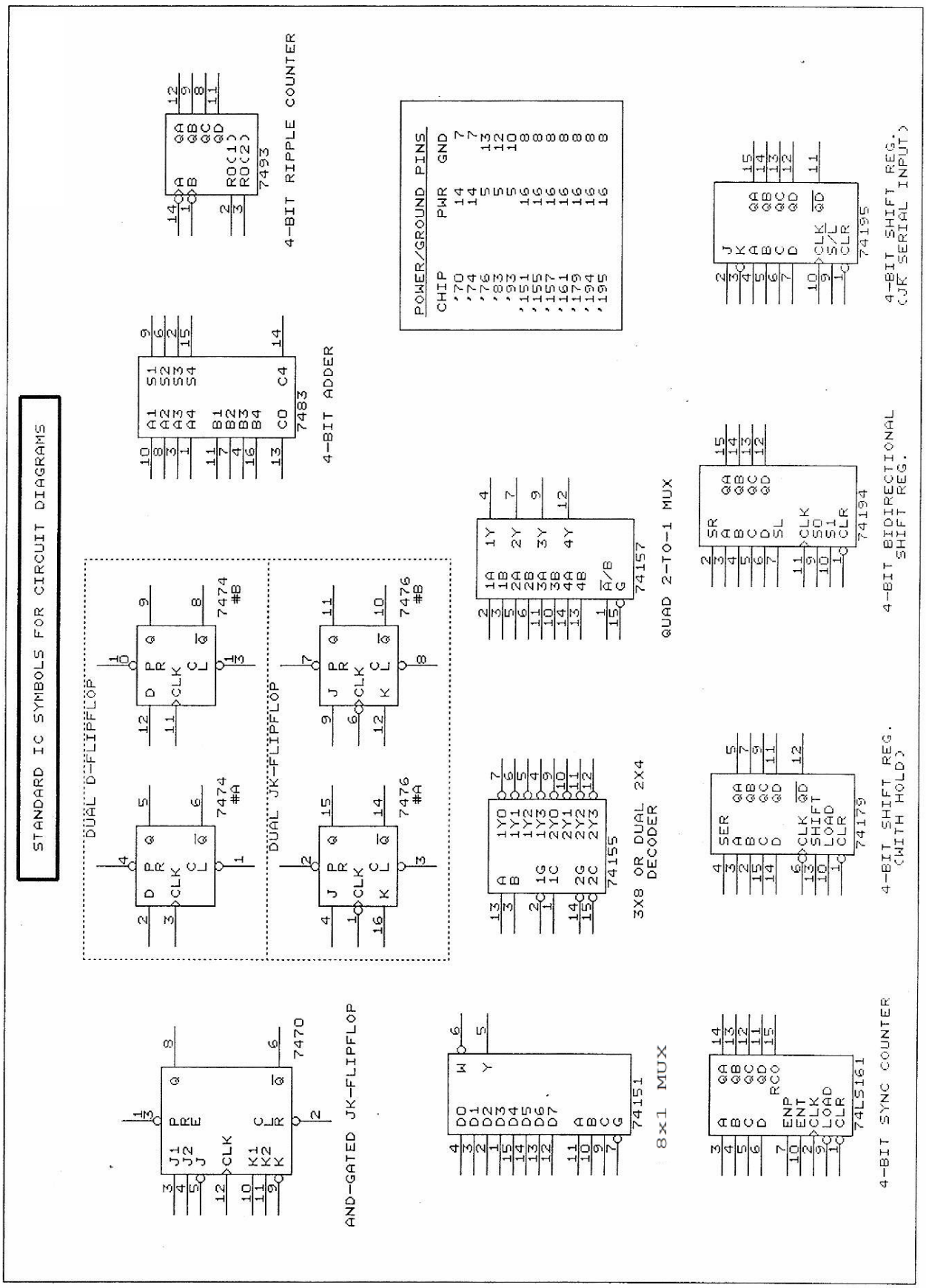
Also, instead of just one "D" (serial) input to QA, there are 2 inputs: J and /K. The state of QA after the shift depends on how J and /K are connected. The following function table shows the effects of different combinations of J and /K on the value of QA after a shift:

	/CLR	$S/\overline{L}$	J	/K	CLK	FUNCTION
1	L	X	X	X	X	CLEAR: (QA...QD) <= (0000).
2	H	L	X	X	↑	LOAD: (QA...QD) <= (A...D).
3	H	H	L	L	↑	SHIFT: (QA,QB,QC,QD) <= (**L,**QA,QB,QC).
4	H	H	L	H	↑	SHIFT: (QA,QB,QC,QD) <= (**QA,**QA,QB,QC).
5	H	H	H	L	↑	SHIFT: (QA,QB,QC,QD) <= (/**QA,**QA,QB,QC).
6	H	H	H	H	↑	SHIFT: (QA,QB,QC,QD) <= (**H,**QA,QB,QC).

When J and /K are the same, QA acts like a D-flipflop (why?) and the next state of QA will be the same as J. This is shown in rows 3 and 6 of the table. So if J and /K were both connected to some external input I, then J = /K = I and, after a shift, QA would have the same value as I. With this connection, the 74195 would act like a 74179.

If J and /K are opposites (i.e. J and K are the same) then QA acts like a T-flipflop. If J is low (row 4), then K is also low and a clock pulse leaves QA unchanged. But if J is high and /K low (row 5), then K is also high and QA toggles with the next clock; i.e. QA → /QA, as the table shows.


PIN ASSIGNMENTS FOR GATE CHIPS
7402 QUAD NOR
7410 TRIPLE 3-INPUT NAND
7400 QUAD NAND
(SAME PINOUT FOR 7408 AND, 7432 OR, 7486 EX-OR)
7404 or 7414 HEX INVERTER
Vcc


STANDARD IC SYMBOLS FOR CIRCUIT DIAGRAMS
DUAL D-FLIPFLOP
7474 #A
7474 #B
DUAL JK-FLIPFLOP
7476 #A
7476 #B
4-BIT ADDER
7483
4-BIT RIPPLE COUNTER
7493
POWER/GROUND PINS
CHIP PWR GND
'70 14 7
'74 14 7
'76 5 13
'83 5 12
'93 5 10
'151 16 8
'155 16 8
'157 16 8
'161 16 8
'179 16 8
'194 16 8
'195 16 8
4-BIT SHIFT REG.
(JK SERIAL INPUT)
74195
QUAD 2-TO-1 MUX
74157
4-BIT BIDIRECTIONAL
SHIFT REG.
74194
3X8 OR DUAL 2X4
DECODER
74155
AND-GATED JK-FLIPFLOP
7470
8x1 MUX
74151
4-BIT SHIFT REG.
(WITH HOLD)
74179
4-BIT SYNC COUNTER
74LS161